Route design methodology

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| Tool Version : Vivado v.2021.1 (win64) Build 3247384 Thu Jun 10 19:36:33 MDT 2021

| Date : Wed Apr 10 16:12:14 2024

| Host : DESKTOP-4LK3EFH running 64-bit major release (build 9200)

| Command : report\_methodology -file UART\_methodology\_drc\_routed.rpt -pb UART\_methodology\_drc\_routed.pb -rpx UART\_methodology\_drc\_routed.rpx

| Design : UART

| Device : xc7z020clg400-1

| Speed File : -1

| Design State : Fully Routed

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Report Methodology

Table of Contents

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1. REPORT SUMMARY

2. REPORT DETAILS

1. REPORT SUMMARY

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Netlist: netlist

Floorplan: design\_1

Design limits: <entire design considered>

Max violations: <unlimited>

Violations found: 20

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| Rule | Severity | Description | Violations |

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| TIMING-18 | Warning | Missing input or output delay | 19 |

| ULMTCS-2 | Warning | Control Sets use limits require reduction | 1 |

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2. REPORT DETAILS

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TIMING-18#1 Warning

Missing input or output delay

An input delay is missing on rd\_uart relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#2 Warning

Missing input or output delay

An input delay is missing on rst relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#3 Warning

Missing input or output delay

An input delay is missing on w\_data[0] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#4 Warning

Missing input or output delay

An input delay is missing on w\_data[1] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#5 Warning

Missing input or output delay

An input delay is missing on w\_data[2] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#6 Warning

Missing input or output delay

An input delay is missing on w\_data[3] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#7 Warning

Missing input or output delay

An input delay is missing on w\_data[4] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#8 Warning

Missing input or output delay

An input delay is missing on w\_data[5] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#9 Warning

Missing input or output delay

An input delay is missing on w\_data[6] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#10 Warning

Missing input or output delay

An input delay is missing on w\_data[7] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#11 Warning

Missing input or output delay

An input delay is missing on wr\_uart relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#12 Warning

Missing input or output delay

An output delay is missing on r\_data[0] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#13 Warning

Missing input or output delay

An output delay is missing on r\_data[1] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#14 Warning

Missing input or output delay

An output delay is missing on r\_data[2] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#15 Warning

Missing input or output delay

An output delay is missing on r\_data[3] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#16 Warning

Missing input or output delay

An output delay is missing on r\_data[4] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#17 Warning

Missing input or output delay

An output delay is missing on r\_data[5] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#18 Warning

Missing input or output delay

An output delay is missing on r\_data[6] relative to clock(s) sys\_clk\_pin

Related violations: <none>

TIMING-18#19 Warning

Missing input or output delay

An output delay is missing on r\_data[7] relative to clock(s) sys\_clk\_pin

Related violations: <none>

ULMTCS-2#1 Warning

Control Sets use limits require reduction

This design uses 2059 control sets (vs. available limit of 13300, determined by 1 control set per CLB). This exceeds the control set use guideline of 15 percent. This is at a level where reduction is REQUIRED (see UG949). Use report\_control\_sets to get more details.

Related violations: <none>